

Novel Quantum Cost Efficient D Flip-Flop and D Latch

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Abstract— a fault tolerant reversible logic has gained Importance as they consume low power and less heat Dissipation. The benefits of logical reversibility can be gained only after employing physical reversibility. Every future Technology will have to use reversible gates in order to reduce Power. In this paper, a new fault tolerant reversible 4*4 RR-gate which satisfies the reversible and parity preserving properties. The D-latch and D-flip flop is designed using proposed 4*4 RR-gate fault tolerant reversible gate. The proposed sequential circuits based on conservative logic gates outperform the sequential circuits implemented in classical gates in terms of testability. Any sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors. The two test vectors are all 1s, and all 0s. The importance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors, thereby eliminating the need for any type of scan-path access to internal memory cells. The proposed design is more efficient than the existing designs In terms of power, delay and power delay product.

Index terms— reversible logic, fault tolerant reversible Logic, fan-out, power, delay, power delay product.

I. INTRODUCTION

According to Landauer's principle, the loss of one bit of information dissipates $kT \ln 2$ joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [4]. Later Bennett, in 1973, showed that in order to avoid $kT \ln 2$ joules of energy dissipation in a circuit it must be built from reversible circuits [5]. In 1965 Gordon Moore observed that the performance of integrated circuit would continue to improve at an exponential rate with the performance per unit cost increasing by a factor of 2, every 18 months. According to Gordon Moore [2], shrinking the dimensions on integrated structures makes it possible to operate the structure at a higher speed for the same power per unit area.

As more and more components are getting packed onto the chip, power dissipation in the present day computer is becoming very high. Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility.

Absolutely perfect physical reversibility is practically unachievable. although the various table text styles are provided. The formatter will need to create these components, incorporating the applicable criteria that follow. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs [4]. Information is lost when the circuit implements nondirective functions. Therefore, in irreversible logic circuit the input vector cannot be recovered from its output vectors. Reversible logic circuit by definition realizes only those functions having one-to-one mapping between its input and output assignments. Hence in reversible circuits no information is lost. Zero energy dissipation would be possible only if the network consists of reversible gates [5].

Perkowski et.al.'s states —every future technology will have to use reversible gates in order to reduce power. This has led many people to pursue research in the area of reversible logic [6]. As all the fault tolerant gates are reversible gates which full fill the reversible logic condition along with the parity preserving fault tolerant property. Fault tolerance enables a system to continue its operations correctly when an error occurs in some parts of it. Detection and correction of errors is so convenient when the components of system are fault tolerant. In communication and many other systems parity will lead to fault tolerance.

ICGPC 2014
St.Peter's University, TN, India.

II. REVERSIBLE LOGIC GATES

A gate is called reversible if there is a one to one correspondence between its input and output patterns. Fan out is not allowed. A logic gate is reversible if the mapping of inputs to outputs is injective, that is, every distinct input pattern a distinct output pattern will be produced, and equal no of input and output are available. Realization of reversible function using gates with smaller width increases the gate count and garbage outputs. Therefore, there must be trade-offs of using a family of reversible gates. There are many reversible gates in the literature. Among them are 2*2 Feynman Gate (FG) [3], 3*3 Peres Gate (PG) [4], 3*3 Toffoli Gate (TG) [7], 3*3 Fred kin Gate (FRG) [8], 3*3 Khan Gate (NG) [7], 3*3 double Gate (F2G) [5], and 3*3 NFT [9]. Any realization techniques should keep both the number of constants and garbage's as low as possible [8]. Garbage Outputs, Constant Inputs, Gate Count, Hardware Complexity, Area Consumption, Path Delay should be made minimum.

III. FAULT TOLEREANT REVERSIBLE LOGIC GATES

Fault tolerance enables a system to continue its operations correctly when an error occurs in some parts of it. Parity checking is one of the widely used mechanisms for detecting single level fault in Communication and many other systems. It is believed that if the parity of the input data is maintained throughout the computation, no intermediate checking would be required [7-8]. Therefore, parity preserving reversible circuits will be the future design trends towards the development of fault tolerant reversible systems in nanotechnology. A gating network will be parity preserving if its individual gates are parity preserving [7]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits. Parity checking is one of the oldest, as well as one of the most widely used, methods for error detection in digital systems. It's most common use is for detecting errors in the storage or transmission of information, primarily because most arithmetic and other processing functions do not preserve the parity of the data. There have been attempts at performing arithmetic operations on specially

Encoded operands in a way that parity checking becomes applicable, but such methods need further development and are not in widespread use [8]. Detection and correction of errors is so convenient when the components of system are fault tolerant.

A reversible logic circuit design should be optimized for following criteria:

- minimum number of reversible gates
- minimum number of garbage outputs
- minimum number of constant inputs
- minimum quantum cost of circuit

We first note that of the gates depicted; only the Fredkin gate is parity-preserving. This is readily verified by comparing the input parity $A \oplus B \oplus C$ (or $A \oplus B$ for the Feynman gate) to the output parity $P \oplus Q \oplus R$ (or $P \oplus Q$). The Feynman gate is quite useful, but, unfortunately, it is inadequate for the synthesis of efficient reversible circuits. Given that synthesis methods with the Toffoli gate, using Fredkin gates to assist in optimizing cost or performance, are quite advanced, we are motivated to look for additional reversible gates that would lead to similarly efficient designs. In this search, the following impossibility result rules out a fundamental role for 2-input, 2-output gates. No 2-input, 2-output reversible gate can be parity preserving. We next look into 3-input, 3-output gates. We have already observed that the Fredkin gate is parity-preserving. Well known fault tolerant gates are [8] New Fault Tolerant Gate, Fredkin gate, Feynman double gate, Islam gate.

A natural question at this point is whether there exist other 3-input, 3-output parity-preserving reversible gates beyond the two depicted. We must perform an exhaustive search to answer this question, but meanwhile have the following preliminary result that indicates such gates, if they exist, would not be of the kinds that lend themselves to simple and efficient design procedures. Up to the permutation of inputs and outputs and (conditional) complementation of outputs Q and R, no 3-input, 3- Output reversible logic gate, other than the two depicted, can be parity preserving if its first output equals its first input ($P = A$). 16 possible ways, if $\{A, B, C\}$ and $\{P, Q, R\}$ are to have the same parity. The output functions Q and R for these 16 cases. It is easily seen that the resulting gate is not useful in four of these cases, is identical to F2G or a variant (F2G-var) in which both Q and R are Complemented in four additional cases, and is identical to FRG. Well known fault tolerant gates are shown in Fig. 1, 2, and Fig. 3.

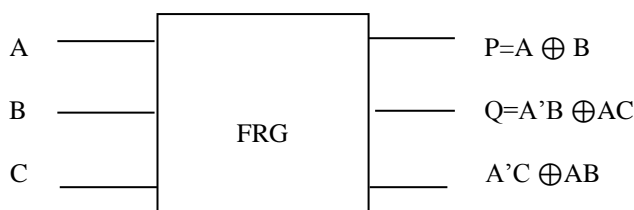


Fig. 1. Fredkin Gate

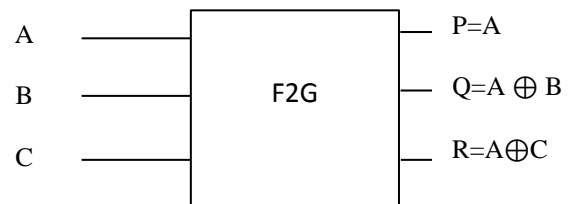


Fig. 2. Feynman Gate

IV. PREVIOUS WORK

In Fredkin gates have been constructed the reversible gates. It uses less no of transistors than conventional CMOS based reversible gates. This reduces the area and as well as to operate the circuit with low power consumption and the speed is increased with the reduction in delay The source of energy supplied to the system is only through the input signals only which will greatly favors' for the future designs.

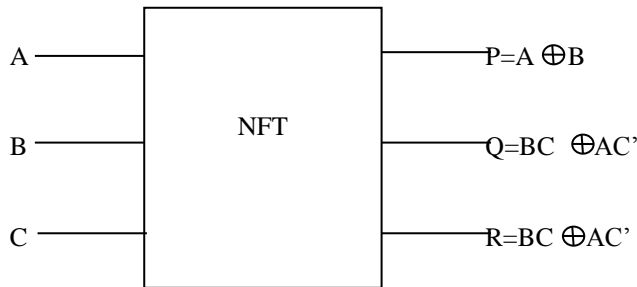


Fig. 3. New fault tolerant gate

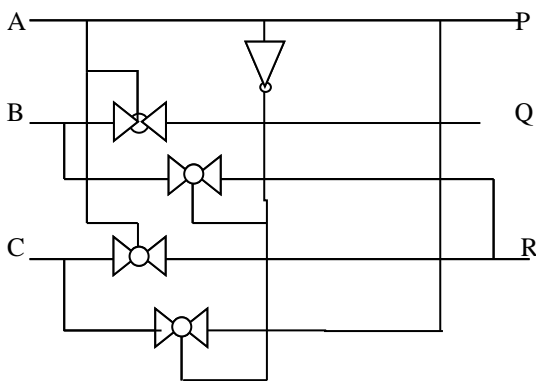


Fig. 4. Transistor form of Fredkin Gate.

V. A NEW PARITY PRESERVING FAULT TOLERANT RR GATES

This paper presents a new 4*4 parity preserving reversible gate, RR Gate (RR), depicted in Fig. 5. The gate is one through, which means one of the input variables is also output. The corresponding truth table of the gate is shown in TABLE I. It can be verified from the truth table that the input pattern corresponding to particular output pattern can be uniquely determined. The proposed reversible RR gate is parity preserving. This is readily verified by comparing the input parity A B C D to the output parity PQRS.

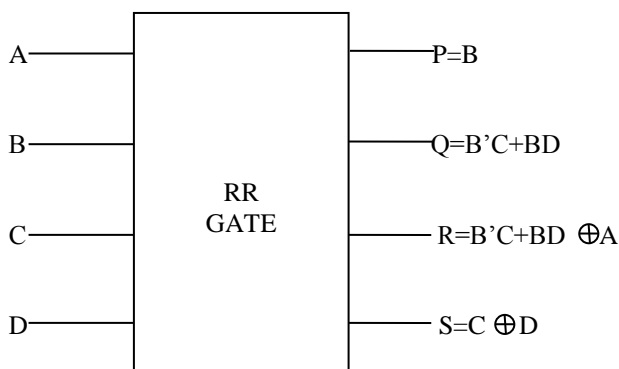


Fig. 5. Proposed RR fault tolerant gate

TABLE I
TRUTH TABLE FOR PROPOSED RR 4*4 FAULT TOLERANT GATE.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	0	1	1	1	1	1
0	1	1	0	1	0	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	1	0
1	0	0	1	0	0	1	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	0	0	1	0	1	0
1	1	0	1	1	1	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

There are other two 4*4 reversible gates in the literature, namely TSG and MKG. Though these two gates are reversible but not parity-preserving and therefore do not allow detection of circuit’s faults.

V. NOVAL DESIGN OF D-LATCH, D-FF USING RR-GATE

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. The D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. The first stage (master) is driven by the clock signal, while the second stage (slave) is driven by the inverted clock signal. Thus the master stage is positive level sensitive, while the slave stage is negative level sensitive. When the clock is high, the master stage follows the D input while the slave stage holds the previous value. When the clock changes from logic “1” to logic “0”, the master latch ceases to sample the input and stores the D value at the time of the clock transition. At the same time, the slave latch becomes transparent, passing the stored master value to the output of the slave stage, Q. This paper provides the design of D-latch DFF using the proposed 4*4 Fault tolerant gate in Fig. 6.,Fig. 7. and Fig. 8.

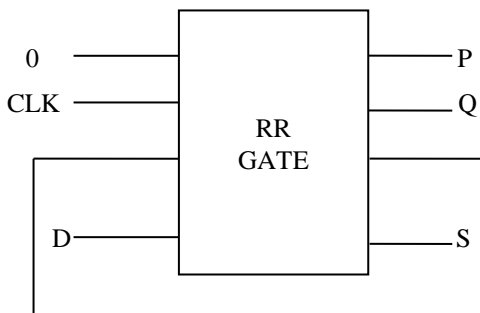


Fig. 6. D Latch using RR Gate

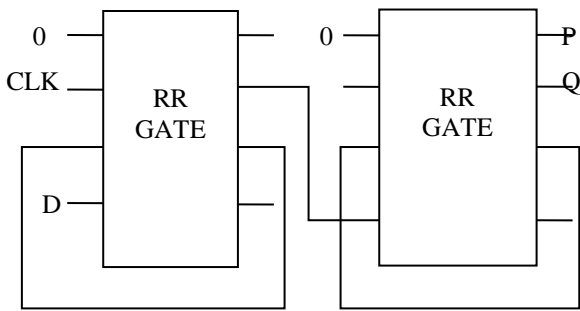


Fig. 7. D Flip Flop Using RR Gate

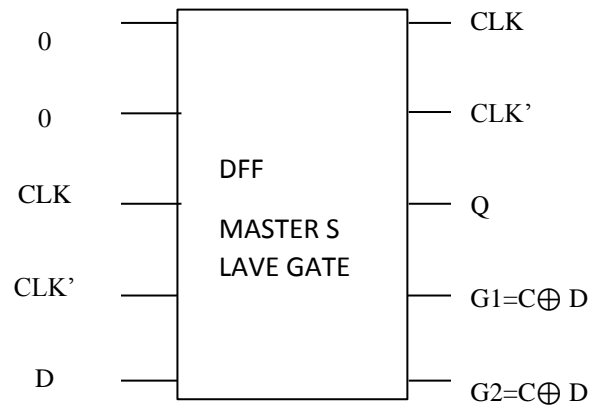


Fig. 8. Master Slave D Flipflop using RR Gate

VII. SHIFT REGISTER

The flip flops are cascaded to form the shift register which shares the same clock, the output of each flip-flop is given as the "data" input to the next flip-flop due to which bit shifting take place. More generally, A shift register may be multidimensional, where data in and data out are in the form of bit array. Several shift register of same length are connected to form this bit array. Shift registers can have both parallel and serial inputs and outputs. These are often configured as serial-in, parallel-out (SIPO) or as parallel-in, serial-out (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. Shift registers are a type of sequential logic circuit, mainly for storage of digital data. As the flip-flops are cascaded the output of one flip flop is provided as the input for other. All flip- flop is driven by a global clock. The available basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. In few lectures, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out. The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

Serial in - Serial out Shift Registers:

The serial in/serial out shift register shown in Fig. 9. accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. The input data is then applied sequentially to the D input of the first flip-flop on the left .During each clock pulse, one bit is transmitted from left to right. The least significant bit of the data has to be shifted through the register from DFF-RRG0 to DFF-RRG3.In order to get the data out of the register; they must be shifted out serially. This can be done destructively or non-destructively. All flip-flops are reset to zero such state is called destructive state. A basic four-bit shift register can be constructed using four D flip-flops. The operation of the circuit is as follows. Depending on the clock the bit shifts from left to right at every clock transaction.

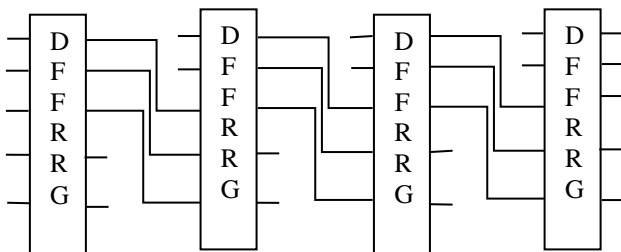


Fig. 9. Serial in serial out.

Serial in - Parallel out Shift Registers:

Data input are provided serially only at the first flip-flop and output is driven parallel .the output of the first flip-flop is provided as the input for the next flip-flop. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. The design of a four-bit serial in - parallel out register is shown in Fig.10.

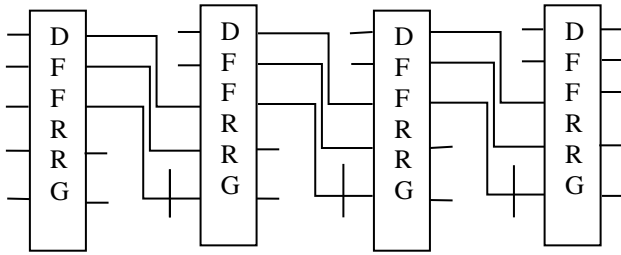


Fig. 10. Serial in Parallel out.

VIII. RESULT AND DISCUSSION

The proposed parity preserving reversible RR and DFF circuits are more efficient than the existing circuits. The proposed circuits can be easily compared with the help of the comparative results given in TABLE II and TABLE III.

TABLE II

D LATCH COMPARISON OF NUMBER OF GATE, CONSTANT OUTPUT, QUANTUM COST, GARBAGE OUTPUT FOR FREDKIN GATE AND GATE

Methods	No. of Gates	No. of Constant input	Quantum cost	Garbage output
Single edge trigger latch using fredkin gate	2	2	14	3
Single edge trigger latch using RR gate	1	1	9	0

TABLE III

D FLIP FLOP COMPARISON OF NUMBER OF GATE, CONSTANT OUTPUT, QUANTUM COST, GARBAGE OUTPUT FOR FREDKIN GATE AND GATE

Methods	No. of Gates	No. of Constnt input	Quant m cost	Garbage output
Single edge trigger latch using fredkin gate	6	6	14	5
Single edge trigger latch using RR gate	2	2	9	2

IX. CONCLUSION

We have given an overview of the k*k parity preserving reversible gates. An efficient Fault tolerant reversible logic RR-gate circuit has been presented. This paper presents a novel realization of fault tolerant reversible D-LATCH, D-FLIPFLOP, SHIFT REGISTER. The number of gates, quantum cost, constant output, garbage output is compared with existing and proposed system. From the tabulation it is very clear that the proposed design is far better than the existing design in all terms.

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